Analytical analysis of Quasi-Saturation Effect in PT and NPT IGBTs

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Abstract—During the turn-on process insulated gate bipolar transistors (IGBTs) traverse a quasi-saturation region from the off-state to the on-state (saturation). The additional voltage drop due to the quasi-saturation of the junction hardly depends on the DC-link voltage. Even if this voltage drop is low comparing to the DC link voltage, the losses due to this effect are rather big as its time constant is large for high-voltage high-speed IGBTs. Standard ZCS or ZVS circuits can't help to avoid those losses. The voltage tail will be analysed in detail for Punch-Through and Non-Punch-Through IGBTs for hard switching on an inductive load. Analytical results will be compared to 2D-simulation and measurements . The dependency of the voltage tail to the doping profile near the junction will be discussed.

In order to minimise the size and weight of inductors and transformers, switching frequency increase is expected, especially at high voltages. But we will show that when the switching frequency exceeds some kilo-hertz the on-state voltage drop may never reach the static value and the on-state losses are much bigger than expected.

I. INTRODUCTION

Power Electronic circuits are widely used for power conversion as they keep good efficiency for a minimal weight in many low to high power applications. Insulated gate bipolar transistors (IGBTs) have many attractive features as a low on-state voltage drop, high current and increasing blocking voltage capabilities. 5kV devices are now being tested and 3.3 kV / 1200 A devices are commercially available.

Apart from the mentioned advantages IGBTs keep high switching losses at hard switching with inductive load. At high switching frequencies those losses may exceed on-state losses and components have to be added to standard power converters to achieve ZVS or ZCS and keep a high efficiency in the system. High performance IGBT models and a good understanding of switching phenomena are required by circuit designers to predict circuit behaviour and to improve the design [1].

The losses due to the voltage tail at turn-on may be very important [2], they will be analysed in detail for PT and NPT IGBTs.

During the following analysis, the IGBT works in a hard-switching configuration with inductive load (fig. 1).

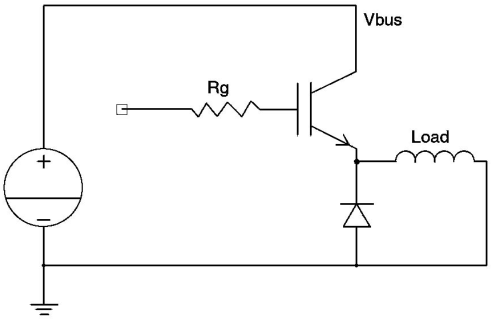

Fig. 1: Hard-switching test circuit.

II. Physical description

In this section the turn-on process of an IGBT will be described in detail.

Neglecting the internal parasitic npn transistor, an IGBT can be approximated by a power pnp bipolar transistor with low current gain driven by a power MOSFET (fig. 2).

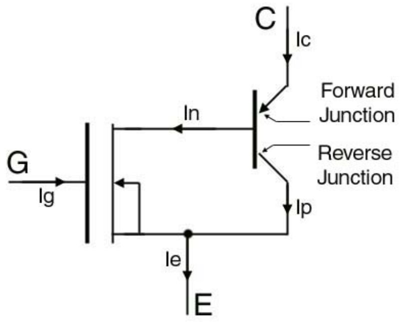

Fig. 2: Simplified IGBT equivalent circuit.

In a normal operating mode the collector potential is always higher than the emitter potential. Then the collector-base junction is always forward biased and the base-emitter junction supports the total blocking capability of the IGBT. When a high voltage is applied on the collector and the gate voltage is low the n-base is partially or totally depleted.

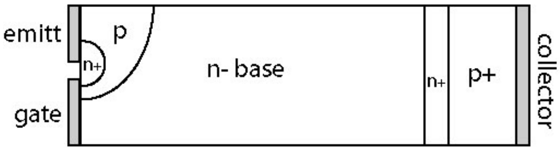

Fig 3: Basic NPT-IGBT doping structure.

Theoretically three different time constants can be observed on the collector-emitter voltage during the turn-on (Fig. 4).
i. a constant slope due to the discharge of the Miller capacitance.
ii. a fast exponential decrease of the base resistance by electron refilling.
iii. a slow exponential decrease of the base resistance and of the emitter-base voltage drop.

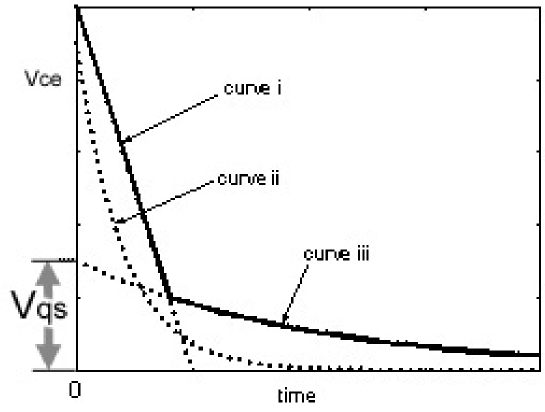

Fig 4: Definition of the quasi-saturation voltage Vqs.

Practically the electron refilling time constant is shorter than the recovery time of a diode and won't appear in hard switching measurements.
The quasi-saturation voltage Vqs is defined as the initial voltage condition of the slow exponential decrease (curve iii).

The depleted region has only a few carriers in the conduction gap and then a high resistance.
When the gate is turned on an electron channel appears under the gate oxide and the depleted region is quickly refilled with electrons (high electrical field in the depleted region). Then a current is allowed to flow through the base.

As no electrons are allowed to flow through the emitter-base junction ($V_{base}>V_e$) a small part of the depleted region near the junction is refilled with holes but not with electrons. This results in a space charge layer and a voltage drop on the junction.

The base is also still not fully modulated and holes have to be injected from the collector to achieve good saturation. Due to the low electrical field in the forward biased collector-base junction the hole injection is slow and it may take microseconds to refill largely depleted layers.
The limited conductivity of the base [3] is generally written as:

$$\begin{aligned}\sigma(x) &= \sigma_p(x)+\sigma_n(x)\\ &= e\cdot\mu_p\cdot p(x)+\left|e\cdot\mu_n\cdot n(x)\right|\end{aligned} \tag{1}$$

and quickly increases for the electrons but not for holes, which leads to unexpected voltage drop across the base. This effect depends on the collector current, but the induced voltage drop on the base is small compared to the voltage drop on the emitter-base junction.

III. Analytical analysis

The diffusion process results in a complex doping profile. The base (n substrate) has basically a constant doping, but the diffused emitter doping profile looks like a gauss function (Fig. 5).

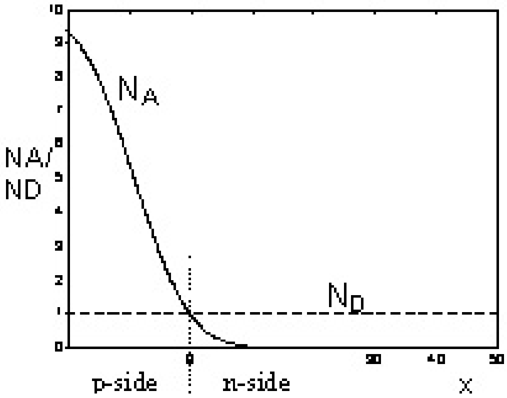

Fig 5: IGBT emitter-base junction doping profile

The exact solution of the Poisson equation leads to a complex equation set. Assuming that the depletion layer mainly extends in the n-side of the junction ($N_A >> N_D$) the doping profile can be approximated by a linear ($N_A - N_D = -kx$) doping on the p-side and a constant doping on the n-side of the junction.

The exact analysis of the value of V_{qs} leads to complex analysis of the geometry and the electron current paths through the base.
It was found that it can be approximated by a function of the electrical field at the junction when the transistor is off E_0:

$$V_{qs} \cong \frac{\varepsilon (E_0)^2}{2eN_{Aeff}} + Uc \qquad (2)$$

where Uc is the ohmic drop in the undepleted base and across the parasitic series resistance and N_{Aeff} is the effective doping on the p-side.

A. NPT IGBTs

In Non Punch-Through (NPT) IGBTs the n-base is large enough so that the depletion layer of the base-emitter blocking junction never reaches the collector side of the substrate.

The Poisson equation on the p-side of the junction ($N_A > N_D$) is [3]:

$$E(x \le 0) = \frac{e}{\varepsilon} \int_{-x_p}^{x} k\xi \cdot d\xi = \frac{ek}{2\varepsilon}\left(x^2 - x_p^2\right) \qquad (3)$$

and on the n-side:

$$E(x \ge 0) = \frac{eN_D}{\varepsilon} \int_0^x d\xi + E(0) = \frac{eN_D}{\varepsilon}(x - x_n) \qquad (4)$$

The total voltage drop on the junction is:

$$V(x_n) = \int_{-x_p}^{x_n} E(\xi) d\xi = \frac{ek}{3\varepsilon} x_p^3 + \frac{e}{2\varepsilon} N_D x_n^2 \qquad (5)$$

Using the global neutrality of the junction (continuity of the electrical field) the total voltage drop can be expressed as a function of E_0:

$$V_{bus} = \frac{\varepsilon}{2eN_D} E_0^2 + \sqrt{\frac{8\varepsilon}{9ek}} \left(\left|E_0\right|\right)^{1.5} \qquad (6)$$

Assuming that the current is mainly provided by the internal MOSFET and the parasitic collector capacitance ($E_{depl} >> E_{cap}$) the voltage drop on the bipolar junction at the beginning of the quasi-saturation region is given by relation (2). Then

$$\begin{aligned} V_{bus} &\cong \frac{N_{Aeff}}{N_D}\left(V_{qs} - Uc\right) \\ &+ \frac{4}{3}\left(\frac{2eN_A^3}{\varepsilon k^2}\right)^{0.25} \left(V_{qs} - Uc\right)^{0.75} \end{aligned} \qquad (7)$$

A numerical solution is required to express V_{qs} as a function of the bus voltage V_{bus}.

The equation (7) shows the dependencies between the DC link voltage V_{bus} and the start point voltage value of the voltage tail V_{qs}.

For comparison the electrical field at the junction E_0 in a reverse-biased abrupt junction is:

$$E_0 = \sqrt{\frac{2e}{\varepsilon} \cdot \frac{N_A N_D}{N_A + N_D} \cdot V_{bus}} \qquad (8)$$

And the voltage drop at the beginning of the quasi-saturation region is:

$$V_{qs} \cong \frac{N_D}{N_A} \cdot V_{bus} + Uc \qquad (9)$$

In the following graph V_{qs} represents the voltage value at the beginning of the exponential decrease.

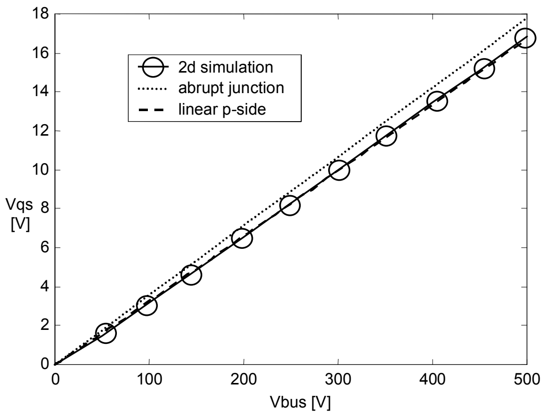

Fig 6: Importance of the voltage tail effect depending on the bus voltage for a NPT-IGBT. Comparison between a 2D Genesise simulation and calculation

This value has been simulated with a finite element method for different source voltages (constant load current) and is compared to the analytical prediction calculated using equation (7) and (9). Just as an indication, this intensive calculation has been done on a Sun server and takes several days of processing for 10 points on the indicated curves

All three calculated curves indicates the same strong increases up to 18 Volts with the DC link voltage up to 500 Volts.

The bigger the blocking collector-emitter voltage is, the larger the inversion layer in the semiconductor is. So it will take much longer to get good saturation in the pn junction with high bus voltages.

B. PT IGBTs

In Punch-Through (PT) IGBTs the depletion layer reaches a n^+ buffer with a higher dE/dx and the depletion width is limited.

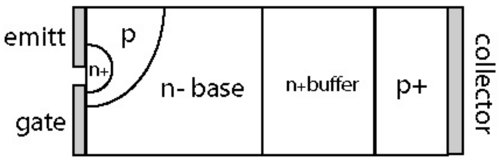

Fig 7: Basic PT-IGBT doping structure

For an increasing reverse polarisation, as long as the depletion layer does not reach the n^+ buffer ($w_{depl}<w_{base}$) the IGBT still acts as a NPT-IGBT. After that limit the electrical field in the depleted layer becomes trapezoidal.

Neglecting the electrical field portion in the buffer layer ($N_{n+} >> N_n$)) the total voltage drop can be expressed as a function of the electrical field at the junction E_0:

$$V_{bus} = w_b E_0 - \frac{eN_D w_b^2}{2\varepsilon} + \sqrt{\frac{8\varepsilon}{9ek}}\left(|E_0|\right)^{1.5} \qquad (10)$$

where w_b is the width of the base.

The voltage at the beginning of the quasi-saturation region still is given by relation (2). Then equation (10) becomes:

$$V_{bus} = \sqrt{\frac{2eN_A w_b^2}{\varepsilon}\left(V_{qs}-U_c\right)} - \frac{eN_D w_b^2}{2\varepsilon} + \frac{4}{3}\left(\frac{2eN_A^3}{\varepsilon k^2}\right)^{0.25}\left(V_{qs}-U_c\right)^{0.75} \qquad (11)$$

In the following graph V_{qs} represents the voltage value at the beginning of the exponential decrease. This value has been measured on a physical device for different source voltages and is compared to analytical prediction calculated using equation (11).

For that calculation doping concentration and inside dimensions have been extrapolated from a specific experimentation set.

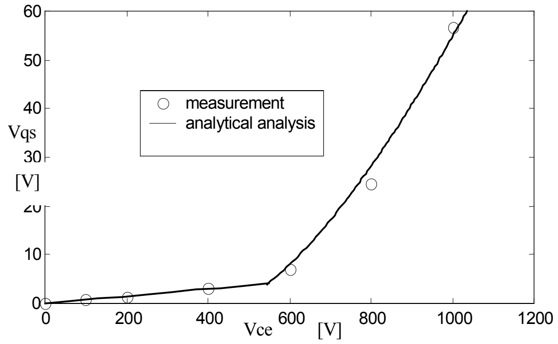

Fig 8: Importance of the voltage tail effect depending on the bus voltage for a PT-IGBT. Comparison between calculation and measurement in 1.2kV ultrafast IGBT IRG4PH50U with Ic=10A and T=25°C.

This effect drastically increases with the DC link voltage.

IV. Dynamic behaviour

As the phenomenon was described in the previous chapter the internal pnp bipolar transistor is always in its normal operating mode and no electrons can flow through its base-collector junction (base-emitter of the IGBT). Then the on-state (Vce_{sat}) of the IGBT should correspond to the calculated Vqs.

This will effectively happen if the internal design and doping profiles leads to a negligible bipolar current gain. The IGBT will be reduced to a power MOSFET with a diode in series, getting a high blocking capability but also a high on-state voltage.

The decrease of Vqs can be explained through the parasitic npn transistor of the IGBT (fig. 9).

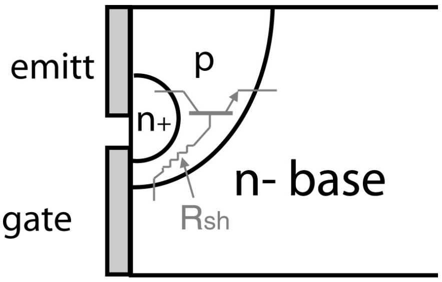

Fig 9: Parasitic npn bipolar transistor

It is well-known that even with a small resistance R_{sh} latch-up may occur and the IGBT will not be controlled by the gate voltage anymore [5]. So the design must minimise the shunt resistance R_{sh} and npn transistor effect.

Unfortunately this parasitic transistor is the only way to refill the base emitter junction with electrons. Due to avoidance of latch-up there are three kinds of electron current allowed.

a) The reverse current I_s of the emitter-emitter pn^+ diode [3].

$$I_s \cong \frac{eAn_i^2 D_p}{L_p N_D} \tag{12}$$

With the high doping needed on the MOSFET source and its small area this current will never exceed some picoAmps.

b) Because of the electrical field remaining in the depleted region the generation ratio is bigger than the recombination ratio. The generated hole current is negligible compared to the bipolar hole current but the generated electron current helps to refill the depleted layer. This current may reach some nanoAmps and it of course hardly depends on the operating temperature.

c) A part of the collector-emitter current traverses the region which is already slightly refilled and accelerates the final step to full modulation.

Then the build-up of electrons in the undepleted base-emitter junction depends on the total electron current through the emitter-base junction $I_{n(be)}$:

$$I_{n(be)} = \frac{dQ(t)}{dt} + \frac{Q(t)}{\tau_n} \tag{13}$$

and

$$Q(t) = I_{n(be)} \tau_n (1 - e^{-t/\tau_n}) \tag{14}$$

It may take thousands times the carrier lifetime τ_n to refill the undepleted junction.

A ZVS will not help to reduce the refilling time. The base-collector junction will block the voltage drop due to the voltage tail and the voltage tail reappears when a current starts to flow through the IGBT.

V. CONCLUSION

Using high speed IGBTs at high voltage to reduce turn-on losses in hard switching applications may drastically increase losses due to the voltage tail.

This effect is also important in quasi resonant converters which are expected to work in the medium frequency range.

In addition to device optimisation and ZVS or ZCS circuits, which about eliminates turn-on and turn-off losses but not losses due to the voltage tail, new circuits have to be designed to reduce the quasi-saturation effect.

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